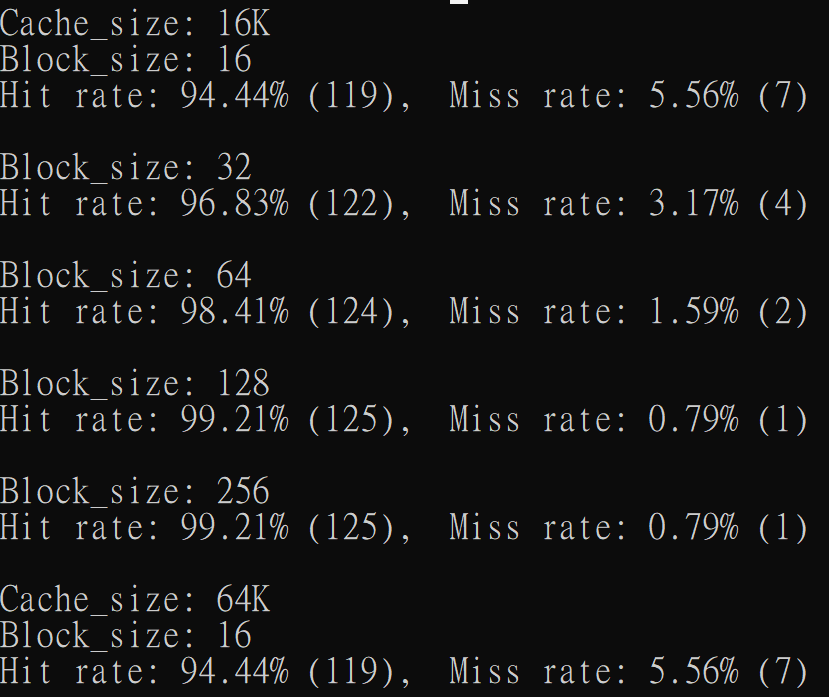
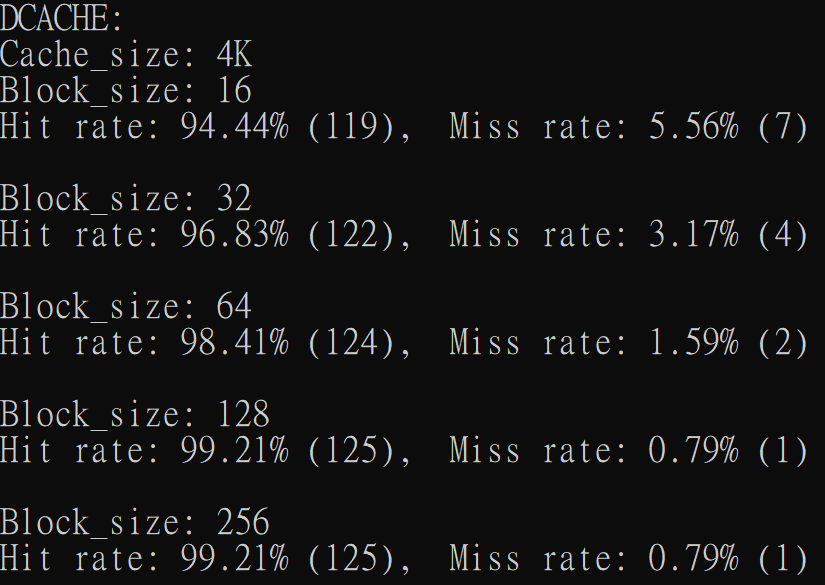
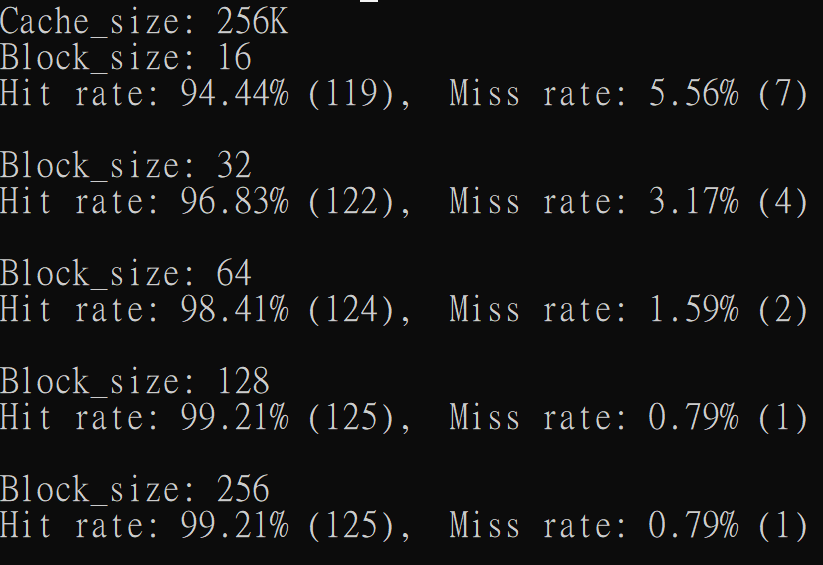
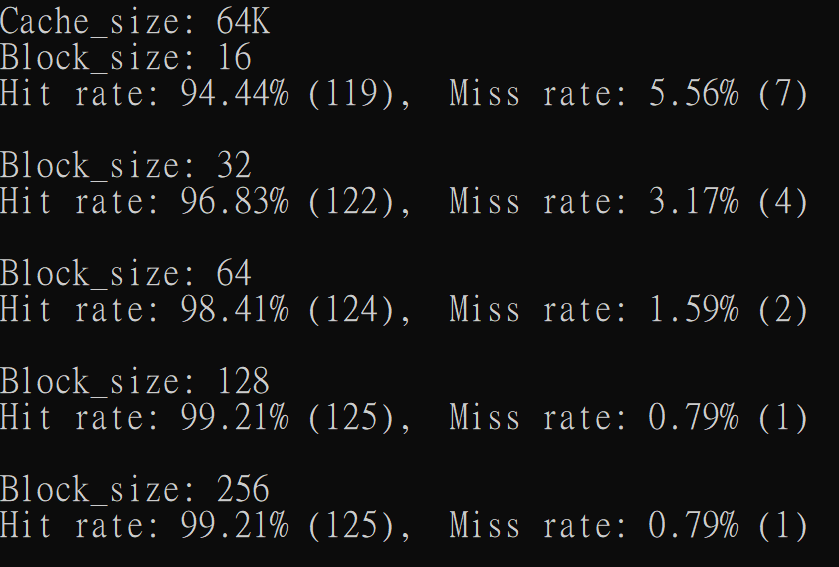
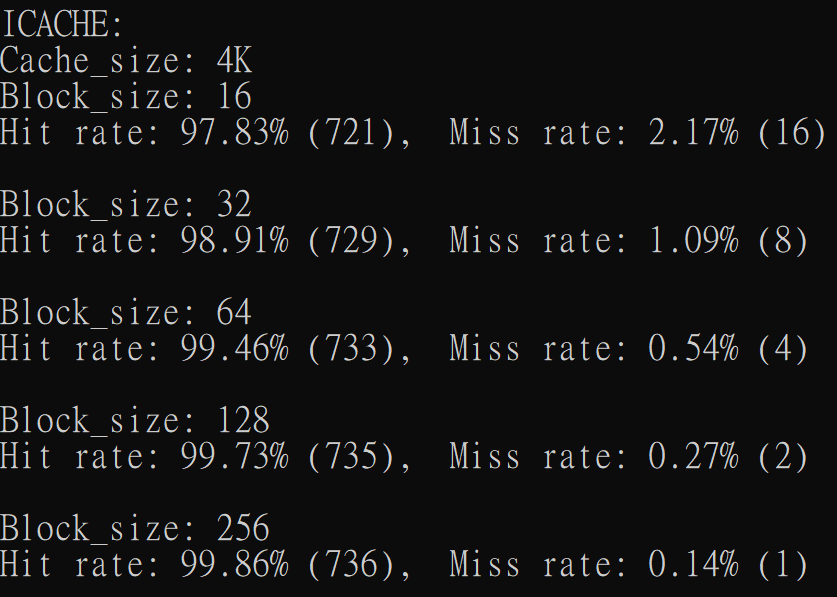
**Direct Mapped Cache**  
- output result

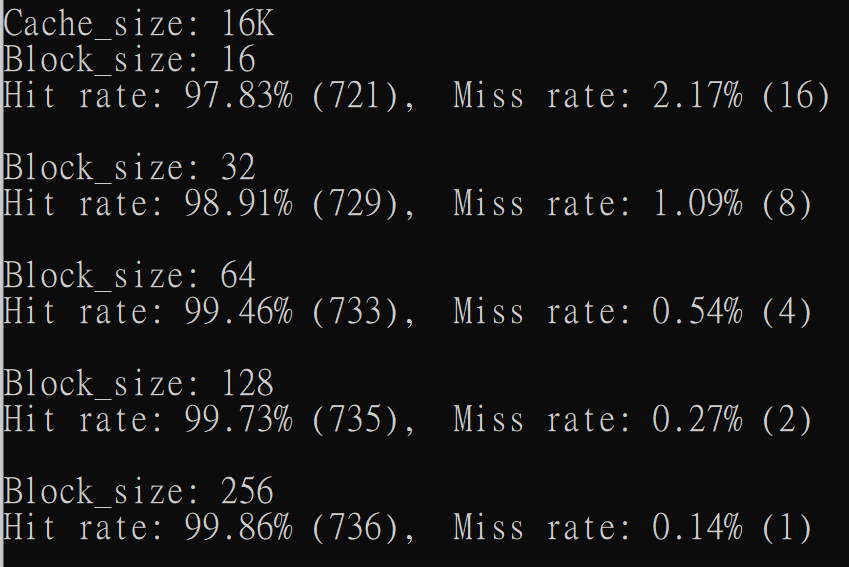
※D-cache

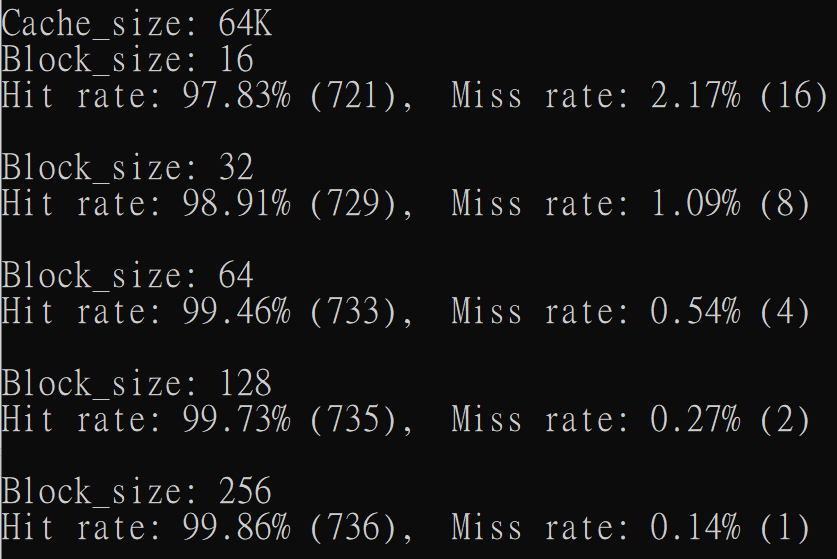


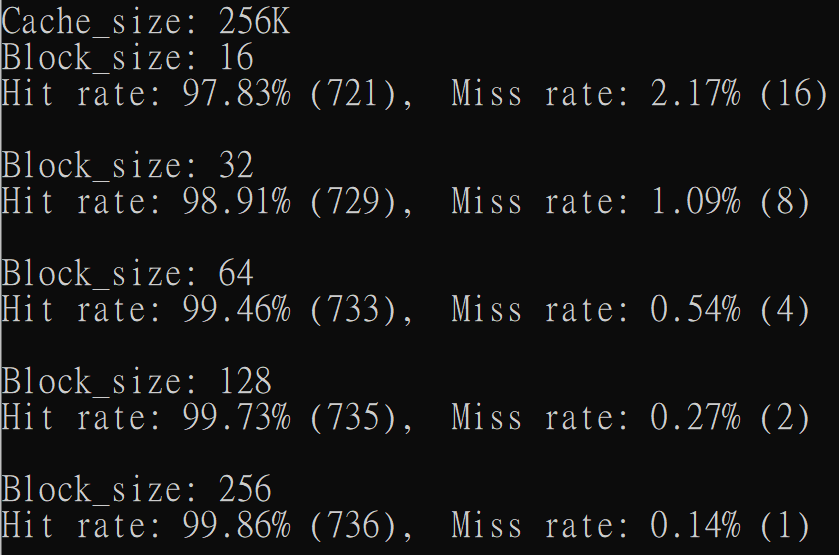


※I-cache

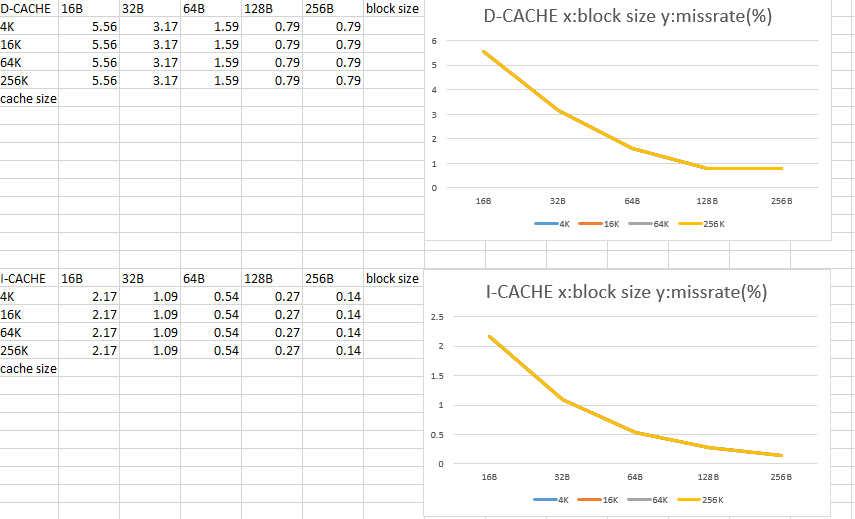








- draw graph and describe the reason for rise and fall

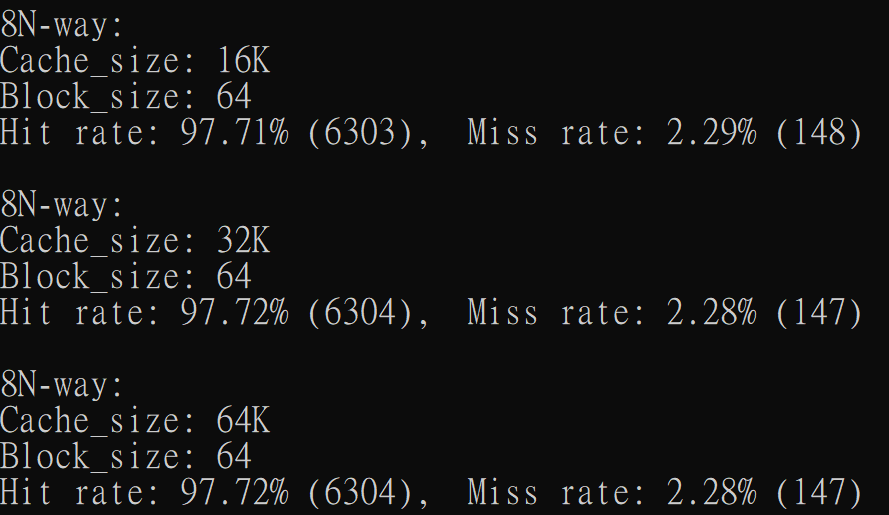
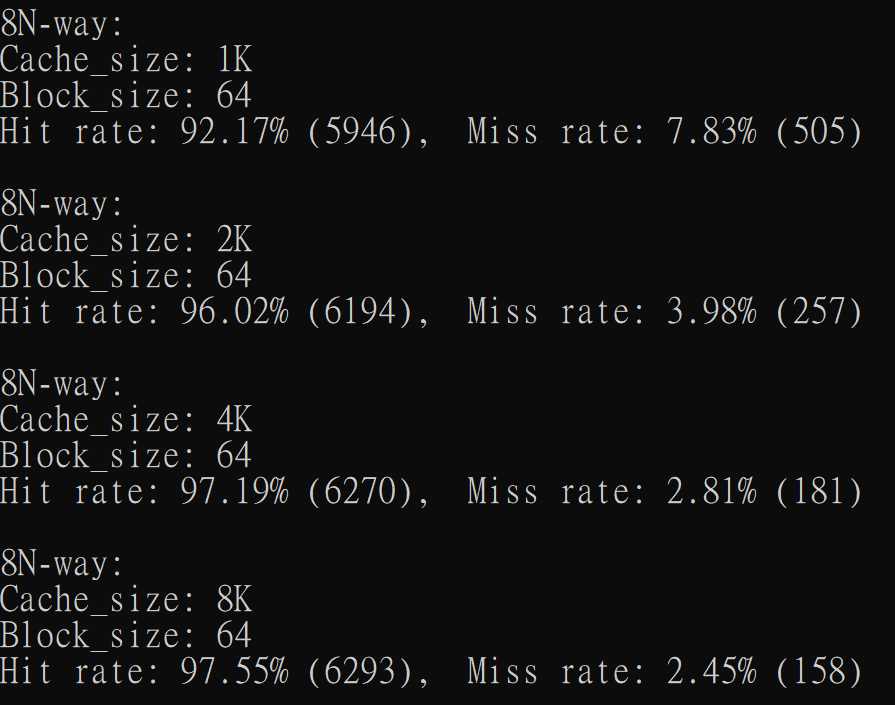
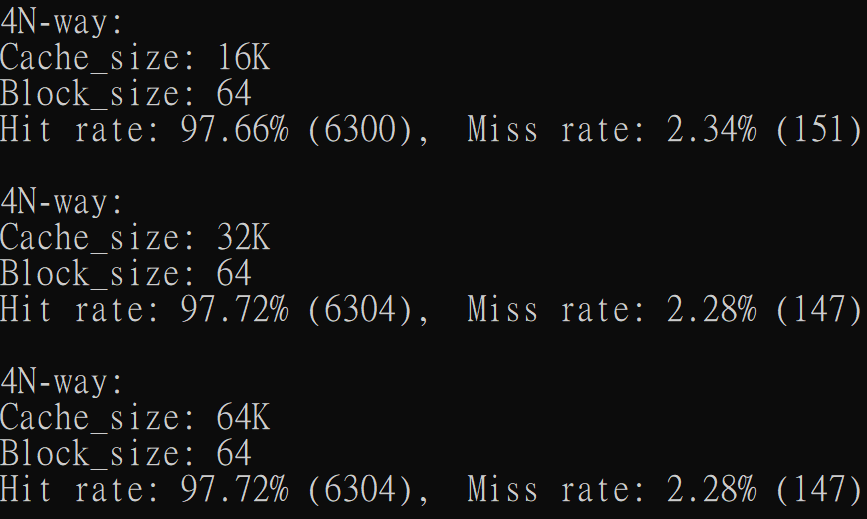
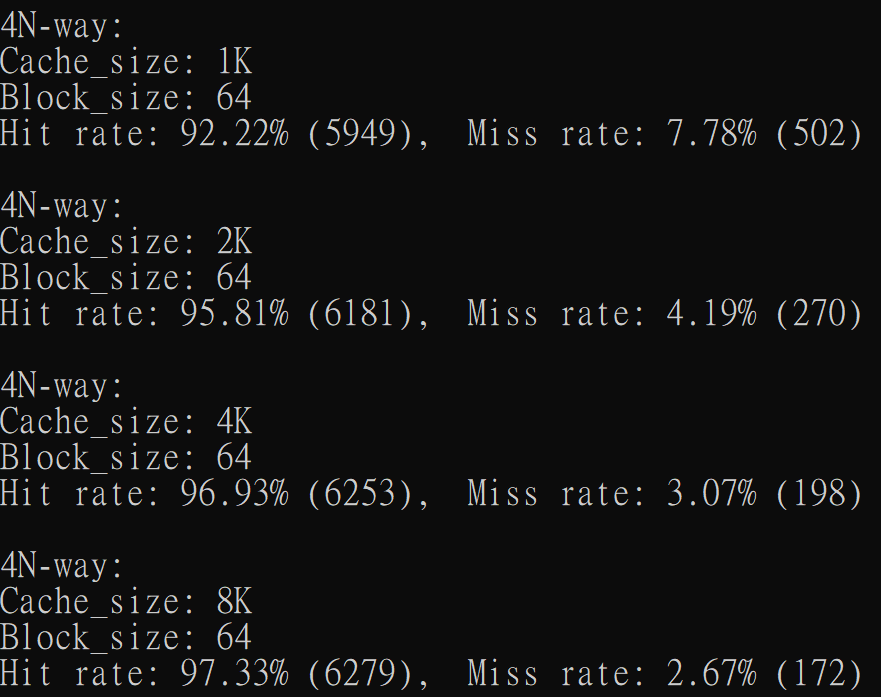
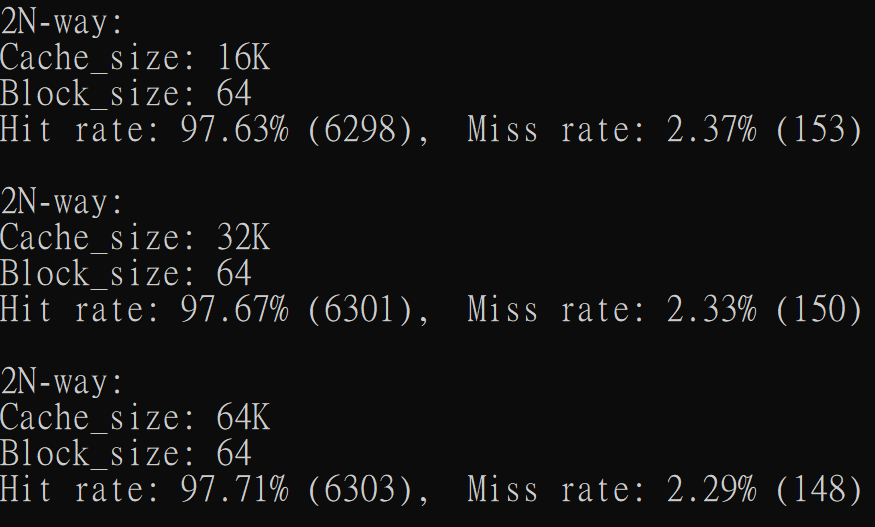
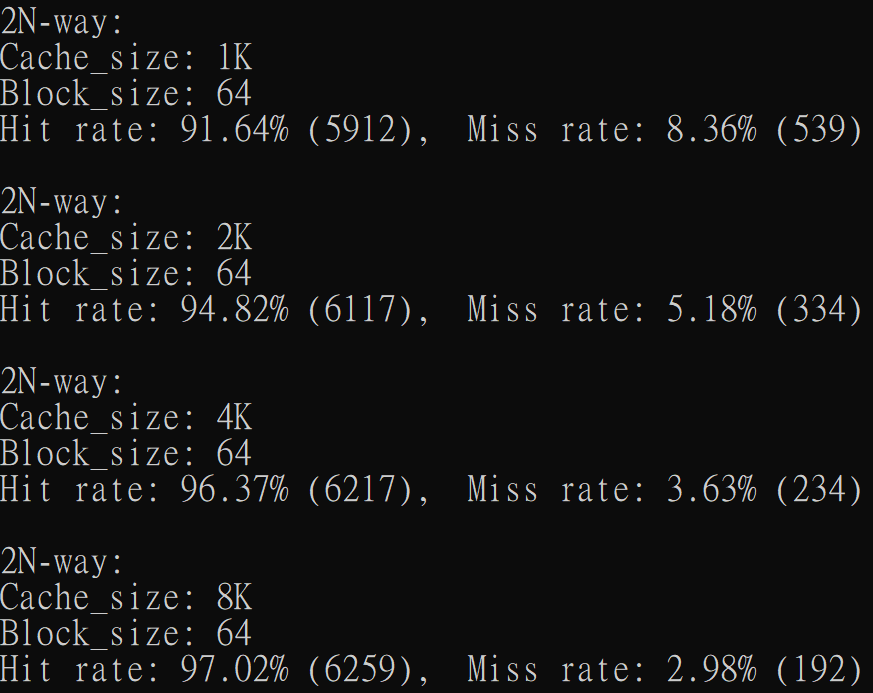
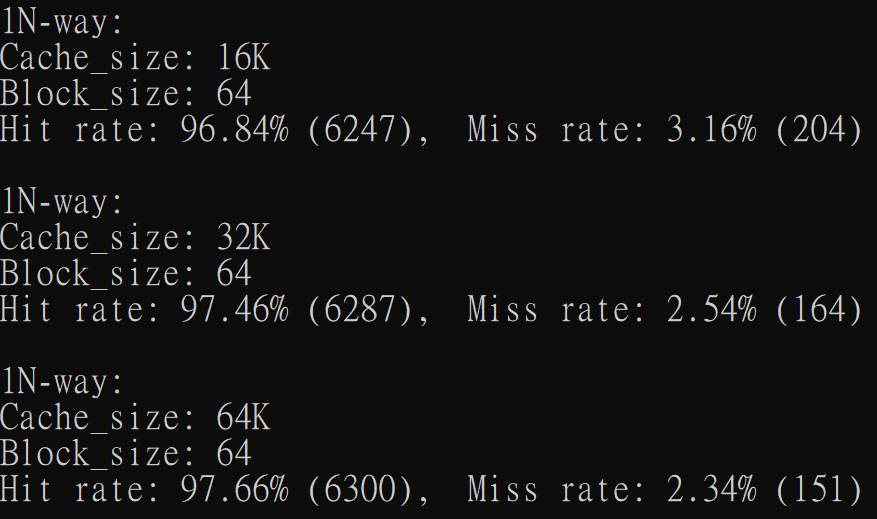
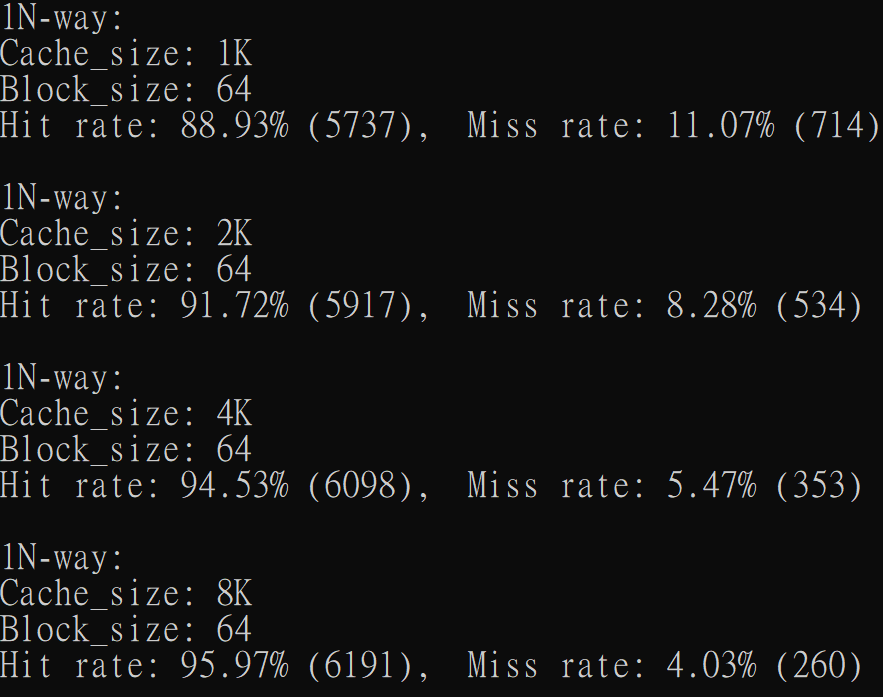


從曲線圖中我們可以發現，隨著block size的增加，miss rate會因為compulsory misses減少而降低。

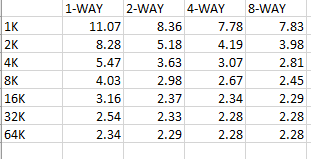
Cache size理論上增加的時候能夠降低capacity miss進而降低miss rate，然而因測資給的值太相近，導致多數都被歸在同一個block中(同index)，所以測不出temporal locality減少所帶來的影響。也因此隨著block size增加，便看不太出 cache size的增加給spatial locality 帶來的提升。

**N-way Set Associative Cache**

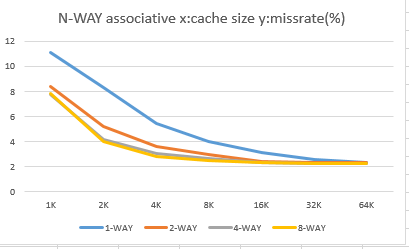
- output result



- table (mention on slide 3)



- draw graph and describe the reason for rise and fall



從摺線圖可以看出來，隨著cache size增加，miss rate逐漸降低，這是因為capacity miss逐漸降低。從N-WAY associative的角度來看，N越大miss rate也逐漸降低，increase associativity可以降低conflict misses。